REMARKS

35 U.S.C. § 103 Rejections

The Examiner has rejected claims 1-12, 16, 29, 30, 32 and 33 under 35 U.S.C. § 103(a) as being unpatentable over Rodder in view of Sekine and Jeuch.

Rodder, Sekine, and Jeuch do not teach or suggest forming an alignment component on a first portion of the substrate, forming silicide regions on a second portion of the substrate, and replacing the alignment component with a conductive gate, the first and second portions of the substrate having the same dopant type after formation of the silicide regions and replacement of the alignment component. Thus, claim 1 clearly defines the first portion of the substrate as being that portion of the substrate over which the alignment component and conductive gate are formed. Likewise, claim 1 clearly describes the second portion of the substrate as being the portion of the substrate over which silicide regions are formed and that these two portions of the substrate have the same dopant type after formation of the silicide regions and replacement of the alignment component.

Rodder teaches a method for forming MOSFET transistors 100 using a disposable gate 120 (Abstract). As shown in Figure 3A, a disposable gate 120 is formed on an active area of the substrate 102 over the region where the channel region of MOSFET 100 is desired (Col. 2, lines 59-64). Raised source-drain regions 106 are formed (Col. 3, line 5). The raised source-drain regions 106 are then doped with an appropriate dopant (Col. 3, lines 21-22). As shown in Figure 3C, an insulator material 114 is then deposited over the structure (Col. 3, lines 41-42). As

shown in Figure 3F, after the disposable gate 120 is removed, an introduction of channel dopants is performed into the channel area 108 of the substrate 102 (Col. 3, lines 66- Col. 4, line 5). As shown in Figure 3G, a gate dielectric 110 is then formed on the channel area 108 followed by the deposition of gate material 126 (Col. 4, lines 11-12). Rodder thus teaches, as clearly illustrated in Figures 3F-3H, forming source and drain regions over undoped portions of a substrate and forming a gate over a doped region of a substrate. Specifically, Rodder does not teach or suggest forming an alignment component on a first portion of the substrate, forming silicide regions on a second portion of the substrate, and replacing the alignment component with a conductive gate, the first and second portions of the substrate having the same dopant type after formation of the silicide regions and replacement of the alignment component.

Sekine teaches fabrication steps of a MOS transistor for forming a sidewall corresponding to a sidewall forming method and for forming corresponding to an application of a salicide technique (Col. 7, lines 40-44). A field oxide film 103 is formed on a P-type or N-type semiconductor substrate 101 (Col. 7, lines 46-47). A gate oxide film 104 is then formed on a transistor-forming region surrounded by the field oxide film 103 (Col. 7, lines 47-51). Next, an amorphous silicon or polysilicon film 105 and a Phospho-Silicate Glass (PSG) film 107 are successively formed on the entire surface of the substrate 101 (Col. 7, lines 51-56). After etching, the polysilicon film 105 and the PSG film 107 which remain become members of the gate electrode (Col. 7, lines 64-65). After the fabrication steps as shown Figures 1A - 1D, an ion

implantation process and a heat treatment are performed for the polysilicon film 105 (Col. 8, lines 27-38). This process increases the existence of the gate electrode and forms a source and drain region 111 (Col. 8, lines 41-43). Therefore, different regions of the substrate are doped differently. Sekine thus clearly teaches differently doped regions under the source and drain regions and the alignment component. Specifically, Sekine does not teach or suggest forming an alignment component on a first portion of the substrate, forming silicide regions on a second portion of the substrate, and replacing the alignment component with a conductive gate, the first and second portions of the substrate having the same dopant type after formation of the silicide regions and replacement of the alignment component.

Jeuch teaches a process for the production of a MIS transistor with a rising substrate/gate dielectric interface wall wherein on the surface of a semiconductor substrate having a given doping type is formed a first electrically insulating layer surrounding a zone of the substrate surface (Abstract). As illustrated in Fig. 5A, the starting point is a type P monocrystalline silicon substrate 40 with a concentration of approximately 10^{16} atoms per cm^3. On the substrate 40 is produced in the conventional manner a SiO_2 field oxide 42 around a zone 44 of the substrate surface in which is called the "active zone" and in which it is wished to create the transistor (Col. 6, lines 18-25). The production of the transistor is completed in the conventional way, as illustrated in Fig. 5I. There is a N-type doping of zones 64 and 66 of the substrate intended to respectively constitute the transistor source and drain, for example, by ionic implantation. Each zone 64 or 66 extends over a depth

of, for example, 250 nm and doping being carried out by arsenic ionic implantation at 100 keV with a dose of, for example, $5x10^{15}$ atoms/cm^2 (Col. 7, lines 36-44). Jeuch thus clearly teaches doping particular regions of the substrate in order to form source and drain regions.

The doping in Jeuch must be performed to form a working transistor. Therefore, if the teachings of Jeuch, in this regard, were to be combined with the teachings of Rodder and Sekine, the resulting transistor would not only have, but require, differently doped regions to form a working transistor.

Specifically, Jeuch does not teach or suggest forming an alignment component on a first portion of the substrate, forming silicide regions or a second portion of the substrate, and replacing the alignment component with a conductive gate, the first and second portions of the substrate having the same dopant type after formation of the silicide regions and replacement of the alignment component.

Claim 1 has been amended to include forming an alignment component on a first portion of the substrate, forming silicide regions on a second portion of the substrate, and replacing the alignment component with a conductive gate, the first and second portions of the substrate having the same dopant type. Specifically, claim 1 includes the limitations "forming an alignment component on a first portion of a substrate of a semiconductor material," "depositing a metal layer over the alignment component and on a second portion of the substrate adjacent to the alignment component, and "replacing the removed alignment component with a conductive gate, the first and second portions of the substrate having the same

dopant type after said formation of the silicide regions and said replacement of the alignment component with the conductive gate."

Therefore, claim 1 is patentable over Rodder in view of Sekine and Jeuch because claim 1 includes a limitation that is not taught or suggested by Rodder, Sekine and Jeuch.

Claims 2-12, 16, 29, 30, 32, and 33 are dependent on claim 1 and should be allowable for the same reasons as claim 1 stated above.

Applicant, accordingly, respectfully requests withdrawal of the rejections of claims 1-12, 16, 29, 30, 32, and 33 under 35 U.S.C. § 103(a) as being unpatentable over Rodder in view of Sekine and Jeuch.

The Examiner has rejected claims 13-15 and 31 under 35 U.S.C. § 103(a) as being unpatentable over Rodder, Sekine, and Jeuch as applied to claim 1 above, and further in view of Inumiya.

Claims 13-15 and 31 are dependent on claim 1 and should be allowable for the same reasons as claim 1 stated above.

Applicant, accordingly, respectfully requests withdrawal of the rejections of claims 13-15, and 31 under 35 U.S.C. § 103(a) as being unpatentable over Rodder, Sekine and Jeuch as applied to claim 1 above, and further in view of Inumiya.

The Examiner has rejected claims 17-19 under 35 U.S.C. § 103(a) as being unpatentable over Rodder, Sekine, Jeuch and Inumiya as applied to claims 1 and 13 above, and further in view of Gardner.

Claims 17-19 are dependent on claim 1 and should be allowable for the same reasons as claim 1 stated above.

Applicant, accordingly, respectfully requests withdrawal of the rejections of claims 17-19 under 35 U.S.C. § 103(a) as being unpatentable over Rodder, Sekine, Jeuch and Inumiya as applied to claims 1 and 13 above, and further in view of Gardner.

The Examiner has rejected claim 28 under 35 U.S.C. § 103(a) as being unpatentable over Rodder, Sekine, and Jeuch as applied to claim 1 above, and further in view of Wolf.

Claim 28 is dependent on claim 1 and should be allowable for the same reasons as claim 1 stated above.

Applicant, accordingly, respectfully requests withdrawal of the rejection of claim 28 under 35 U.S.C. § 103(a) as being unpatentable over Rodder, Sekine and Jeuch as applied to claim 1 above, and further in view of Wolf.

Applicant respectfully submits that the present application is in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call Mark A. Kupanoff at (408) 720-8300.

Pursuant to 37 C.F.R. 1.136(a)(3), Applicant hereby requests and authorizes the U.S. Patent and Trademark Office to (1) treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time and (2) charge all required fees, including extension of time fees and fees under 37 C.F.R. 1.16 and 1.17, to Deposit Account No. 02-2666.

Respectfully submitted,

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